A 2-GHz Subharmonic Sampler for Signal Downconversion

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***Abstract*— Subharmonic sampling is a discrete-time solution to the signal downconversion problem. It can be used either to replace a traditional continuous-time mixer in a superheterodyne receiver or can be combined with other discrete-time analog signal processing blocks in novel receiver architectures. We present a 2-GHz bandwidth integrated mixer based on subharmonic sampling operating at sampling frequencies from 40 MHz to 1.5 GHz. The conversion efficiency is optimized by appropriate choice of the clock duty cycle. The sampler uses a two-diode topology with a 3-V supply. The downconversion loss for the passive sampler is 1 dB and the total system gain 3 dB. The mixer achieves IIP3 of +16-dBm and −1-dB compression +7 dBm for a single-tone input. The circuit was implemented with a 0.6-μm GaAs metal–semiconductor field effect transistor (MESFET) process.**

***Index Terms*—Frequency conversion, integrated circuits, MESFET circuits, MMIC mixers, mobile communication, sampled data circuits, subharmonic sampling.**

I. Introduction

IN THE SAMPLING process, harmonic components, generated in the switching operation, mix with the band-limited input signal and produce replicas over a wide range of frequencies. A replica, located at baseband or close to it, can be used as a downconverted signal in baseband or IF signal processing [1]. Therefore, in comparison to classical continuous-time mixers, an additional degree of freedom for LO frequency selection is available. To prevent aliasing of signal replicas, a sampling frequency at least twice the signal bandwidth must be chosen. By appropriate choice of the switch duty cycle a small conversion loss for a passive structure can be achieved.

To produce the desired IF frequency we can choose from the set of sampling frequencies given by the equation

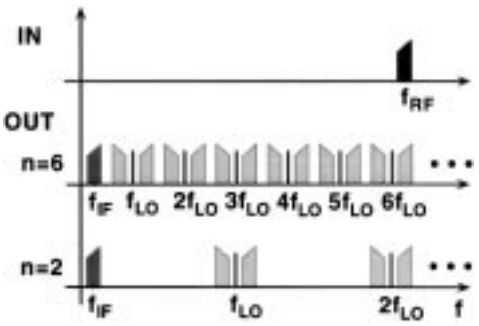

Fig. 1. Spectral behavior of a subharmonic sampler with two different sampling ratios.

$f_{\mathrm{IF}} = \min(|f_{\mathrm{RF}} - nf_{\mathrm{LO}}|)$, where n is an integer called the sampling ratio. In Fig. 1, two different sampling frequencies produce the same IF. The higher sampling frequency produces less harmonic components close to the desired IF. The more significant benefit for using a high sampling frequency comes from the fact that every switching harmonic converts noise around it to baseband. Because one source of the noise is the switch resistance of the sampler, the internal noise aliasing problem can only be reduced by increasing the sampling frequency.

Subharmonic samplers in the RF frequency range have been used up to 1 GHz as a separate mixer [2], as a part of the receiver front-end including filtering [3] and in a picocell wireless terminal prototype [4]. Some recent direct digitization GPS receivers use the same principle in the front-end at 1.5 GHz [5], [6]. In this paper, we demonstrate for the first time a fully integrated subharmonic mixer with an on-chip strobe pulse generation circuit capable of handling input signals up to 2 GHz with small conversion loss and high third-order intercept and compression points. It uses a pair of two-diode bridges and operates with a single 3-V power supply, which is very low for a diode bridge sampler. Our approach uses a relatively high sampling frequency to reduce the noise aliasing problem inherent in subharmonic samplers. The highest available sampling frequency 1.5 GHz is significantly larger than the typical input signal bandwidth of a mobile receiver.

In Section II, we define the conversion efficiency of a subsampling mixer as a function of the duty cycle. The theory is applied in Section III where the circuit design procedure is explained. Special issues in discrete-time mixer measurements including noise are discussed in Section IV. Section V

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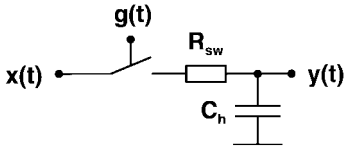


Fig. 2. Sampler model in the analysis.

discusses the measured performance. The work is summarized in Section VI.

II. Conversion Efficiency of a Subsampling Mixer

The conversion efficiency of a subsampling mixer can be obtained from the simplest possible description of a sampler including only the switch resistance and hold capacitor in Fig. 2. The circuit has two operation modes which depend on the switch position. When the switch is closed the output tracks the input and the operation corresponds to first-order low-pass filtering. There is thus no frequency translation. Opening the switch turns the sampler to the hold mode, and the output retains the final value of the input until the switch turns on again. The queue of samples forms a hold envelope in the time domain at the intermediate frequency according to

$$f_{\mathrm{IF}} = |f_{\mathrm{RF}} - mf_s| \tag{1}$$

where m is the harmonic component of the sampling frequency closest to the RF frequency. Thus, the hold mode converts the signal power down to the desired IF by appropriate choice of sampling frequency. Because of fast transients during the changes between two operation modes, the signal spreads over a wide range of frequencies. Theoretically it can be shown that the desired IF component can be designed to be much larger than the unwanted spurious responses thus yielding a small conversion loss for a passive structure. Before that, the following conditions must be met to validate the simple analysis and give the first level design prerequisites. Signal bandwidth is limited to the half of the sampling frequency to avoid spectral aliasing. That is typically done with the preselection filter located directly after the antenna in the receiver front-end. In the circuit, the time constant for charging the hold capacitance must be small compared to the time duration while the switch is closed in order to track the input. The falling edge of the sampling pulse must be steep enough so as not to limit the input bandwidth. The circuit output should be terminated with a high-impedance buffer to minimize signal droop during hold.

In the track mode, the input signal $x(t) = A\cos(\omega_{\mathrm{in}}t)$ is multiplied directly with a rectangular gate function. For a single tone input the output is

$$\begin{aligned} y_{\mathrm{tr}}(t) &= x(t)g(t) = x(t)\cdot\prod\left(\frac{t}{\tau}-\frac{1}{2}\right) \\ &= \frac{x(t)}{T_s}\sum_{k=-\infty}^{+\infty}\left(\int_0^{\tau} e^{-jk2\pi f_s t}\,dt\right)e^{jk2\pi f_s t} \\ &= A\cdot\sum_{k=-\infty}^{+\infty}\frac{\sin(k\pi f_s\tau)}{k\pi}e^{-jk\pi f_s\tau}\cos(\omega_{\mathrm{in}}t)e^{jk2\pi f_s t} \end{aligned} \tag{2}$$

where $T_s = 1/f_s$ is the interval between samples and τ is the width of the pulse. The effect of the hold can be obtained when the rectangular hold function, which is nonoverlapping with the gate function, is convolved with the sampled values taken at the moment when the switch turns off giving

$$\begin{aligned} y_h(t) &= x_s(t) * h(t) \\ &= A\cos(\omega_{\mathrm{in}}t)\cdot\sum_{k=-\infty}^{+\infty}\delta(t-kT_s-\tau) * \prod\left(\frac{t-\frac{T_s-\tau}{2}}{(1-\eta)T_s}\right). \end{aligned} \tag{3}$$

The clock duty cycle $\eta = \tau/T_s$ is taken as a separate parameter used later in the analysis. Track and hold mode waveforms are nonoverlapping in time and therefore the output can be defined by their superposition both in the time domain and in the frequency domain. The Fourier transform of the output is thus

$$\begin{aligned} Y(f) =& Y_{\mathrm{tr}}(f) + Y_h(f) \\ =& \eta\sum_{n=-\infty}^{+\infty}\frac{\sin(n\pi f_s\tau)}{n\pi f_s\tau}e^{-jn\pi f_s\tau}X(f-nf_s) \\ &+ \frac{\sin[\pi fT_s(1-\eta)]}{\pi fT_s}e^{-j\pi fT_s(1+\eta)}\sum_{n=-\infty}^{+\infty}X(f-nf_s). \end{aligned} \tag{4}$$

For the sinusoidal stimulus $x(t) = A\cos(\omega_{\mathrm{in}}t)$ the (4) can be rewritten by using the Fourier transform of the input $X(f) = A\cdot\delta(f - f_{\mathrm{in}})$

$$\begin{aligned} Y(f) = A\eta&\sum_{n=-\infty}^{+\infty}\frac{\sin(n\pi f_s\tau)}{n\pi f_s\tau}e^{-jn\pi f_s\tau}\delta(f-f_{\mathrm{in}}-nf_s) \\ &+ \frac{A\sin[\pi fT_s(1-\eta)]}{\pi fT_s}e^{-j\pi fT_s(1+\eta)} \\ &\times\sum_{n=-\infty}^{+\infty}\delta(f-f_{\mathrm{in}}-nf_s). \end{aligned} \tag{5}$$

To calculate the conversion efficiency at zero IF, i.e., direct downconversion case we have to first define the set of outputs which can produce zero frequency components. It happens only when f_{in} is an integer multiple of the sampling frequency, called m according to (1). We get

$$\begin{aligned} Y(f) = A\eta&\sum_{n=-\infty}^{+\infty}\mathrm{sinc}(nf_s\tau)e^{-jn\pi f_s\tau}\delta(f-(m+n)f_s) \\ &+ A(1-\eta)\mathrm{sinc}[fT_s(1-\eta)]e^{-j\pi fT_s(1+\eta)} \\ &\times\sum_{n=-\infty}^{+\infty}\delta(f-(m+n)f_s). \end{aligned} \tag{6}$$

It produces the replica at dc when $m = -n$ and hence, the downconverted component is

$$Y(0) = A\eta\,\mathrm{sinc}\,(mf_s\tau)e^{jm\pi f_s\tau} + A(1-\eta). \tag{7}$$

When the desired IF is much smaller than half of the sampling frequency, the previous formula approximates the transfer

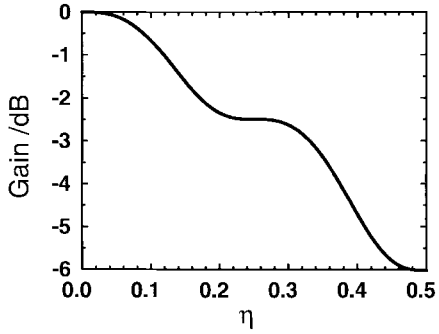


Fig. 3. The theoretical conversion efficiency of a direct conversion sampling mixer as a function of the sampling clock duty cycle at the sampling ratio of 4.

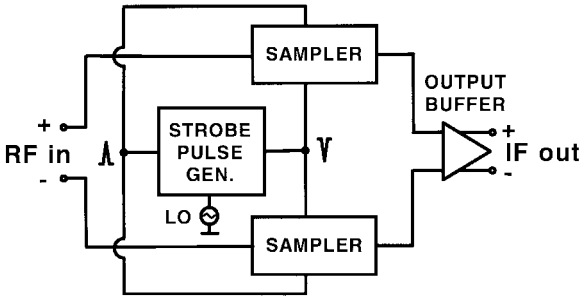


Fig. 4. Block diagram of the circuit. Differential input and output signals are combined after dc isolation by using discrete 180° hybrids in the measurement setup.

function at low intermediate frequencies accurately and simplifies analysis. We define the signal undersampling ratio, or simply sampling ratio, to be

$$n_s = \frac{f_{-3\,\mathrm{dB}}}{f_s} \tag{8}$$

where $f_{-3\,\mathrm{dB}}$ is the highest incoming signal frequency below the sampler −3 dB point which makes n_s integral. Thus, the power conversion efficiency for an arbitrary sampling pulsewidth and ratio is

$$G = \frac{Y(0)Y^*(0)}{X(f_{-3\,\mathrm{dB}})X^*(f_{-3\,\mathrm{dB}})} = (1-\eta)^2 + \frac{(1-\eta)\sin(2\pi n_s \eta)}{n_s \pi} + \frac{1-\cos(2\pi n_s \eta)}{2n_s^2 \pi^2}. \tag{9}$$

The theoretical conversion efficiency is shown in Fig. 3 as a function of the clock duty cycle.

Equation (6) shows that any input frequency located at some harmonic of the sampling frequency will alias down to baseband. The input bandwidth of the sampler limits the noise at high frequencies like a first-order low-pass filter, and the aliasing from external sources is theoretically avoided with the bandpass filter in the receiver front-end. But the noise generated after the filter will be aliased as any other input frequency, and hence the noise performance will deteriorate as a function of the sampling rate. In practical receivers operating in the 1–2 GHz range, the stopband attenuation of the prefilter is far from ideal, and the front-end amplifier introduces noise outside the RF-band as well. In principle, a noise filter in front of the sampler would reduce the previous phenomena, but the noise generated by the switch can not be avoided. Therefore, the noise aliasing is an inherent problem for subharmonic samplers and can be seen in the noise figure performance.

III. Circuit Description

Sampling circuits can be roughly divided to two categories according to the switch type. Diode switches are often used when high-speed switching is needed, but at lower sampling frequencies transistor switches are the dominant choice. Most subsampling mixers use CMOS switched capacitor track-and-hold circuits [2]–[4]. This topology limits the clock frequencies to approximately 100 MHz, and hence, the input bandwidth of the mixer is close to the Nyquist limitation for wireless communication systems like GSM, which has 30 MHz receive bandwidth. Our intention was to use a topology capable of operating at smaller sampling rates in order to reduce the effect of noise aliasing and to minimize the conversion loss. The 2-GHz input bandwidth allows the use of the same mixer for systems like DCS1800 and DECT in addition to the 1-GHz range applications.

The circuit consists of two sampling bridges, an output buffer, and the strobe pulse generation circuit. Fig. 4 shows the block diagram of the downconverter. The differential high-frequency input signal is divided to two separate single-ended samplers which have a common differential buffer in the output. Differential signal processing, although expensive in terms of power, is preferable in RF circuitry because of the insensitivity it provides to common-mode distortion from the substrate and supply voltages. Isolation is very important when high-speed clocks are present in the RF circuitry. In addition to that there is a requirement for separate analog and digital supplies. Although the strobe pulse generation is implemented with differential structures, the top and bottom nodes of the sampling bridge are finally controlled by two separate single-ended pulses which have opposite phases. A slight asymmetry between pulses is inevitable. At small input signal levels, the asymmetry dominates charging the hold capacitor from sample to sample to one direction and thus limiting the dynamic range. With two separate bridges the error cancels out in the output buffer when the differential branches are recombined. The strobe pulses are generated on-chip from an external signal source.

A. Sampling Bridge

Diode bridge design with field effect transistors (FET's) and a low supply voltage has the problem that it requires large amplitude sampling pulses. Schottky diodes are easily implemented in a MESFET process, but the commonly used four diode bridge requires current sources on the top and bottom of the bridge to supply sufficient current during the track mode. Hence, at turn on, two diodes and two current source transistors in saturation are in the stack between the supply rails simultaneously. The minimum saturation voltage of a depletion mode transistor biased at I_{DSS} is close to 1 V in a typical MESFET process. Hence, the smallest possible supply is theoretically 3.4 V. DC isolation between the bridge

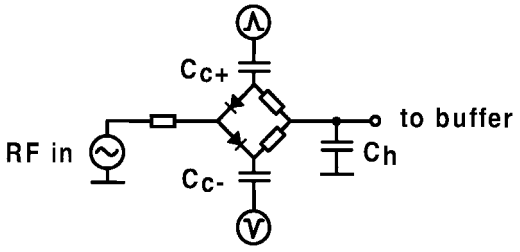


Fig. 5. Two-diode sampling bridge. The hold and coupling capacitance values are all 0.5 pF.

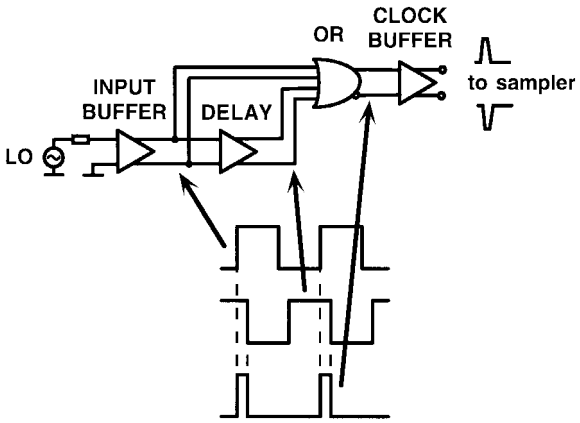


Fig. 6. Strobe pulse generator circuit with timing diagram.

and current sources is not possible because the discharging of the coupling capacitors is too slow while tracking and the continuous charging of the capacitors from sample to sample destroys the operation. The trend toward low supply voltages requires the use of alternative topologies in diode bridge samplers implemented with MESFET technologies.

The two-diode bridge [7] in Fig. 5 is capable of operating with a low supply voltage because the strobe pulse circuit can be dc decoupled. The initial design specification was 3 V, but in the measurements the strobe pulse generator was insensitive to supply variations from 2.7 up to 5 V. The diodes conduct when the sharp strobe pulses pull the voltage over the turn-on point. The current from the pulse generator charges the hold capacitor to a voltage proportional to the input. The falling edge of the strobe turns off the diodes and switches the sampler to hold mode. In the hold mode, the hold capacitor connected to a high impedance buffer keeps its value with a small droop. Simultaneously, the coupling capacitors discharge through the bridge resistors because the output node of the bridge is at a virtual ground for the strobe circuit. The resistors also keep the voltage at the top and bottom of the bridge equal to the output during the hold mode, and therefore no reverse biased bootstrap diodes are needed.

B. Output Buffer

In a subsampling mixer followed by continuous-time circuitry, discharging of the capacitor during the hold mode decreases the conversion efficiency. On the other hand, if discrete-time samples are processed after the circuit the same effect can be handled as a reduced voltage value directly

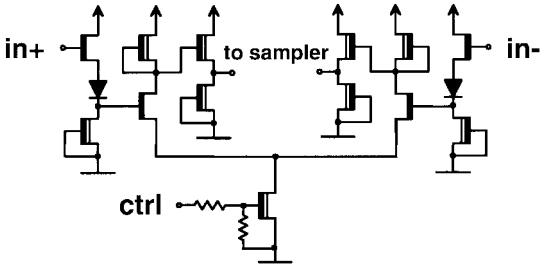


Fig. 7. Schematic of the clock buffer. Strobe pulses are fed to the sampling bridge in Fig. 5 through the coupling capacitors Cc+ and Cc-.

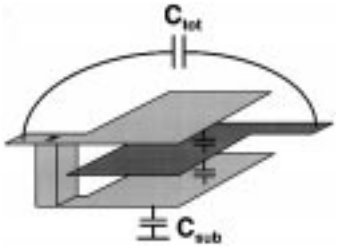


Fig. 8. Capacitors were implemented with three wiring layers to minimize the area and large parasitics to substrate.

proportional to the time constant. In both cases, a high impedance buffer after the sampler is needed to minimize the droop during the hold mode. We used a differential common source amplifier with resistive loads followed by two emitter followers driving the 50-Ω loads in the measurements. A common source stage provides high input impedance and good common mode rejection. The bias to the input transistors is brought through the bridge to avoid discharge through the biasing circuit. The simulated buffer gain is 4 dB.

C. Strobe Pulse Circuit

As seen from Fig. 3, the conversion loss is minimized when an infinitely narrow sampling pulse is used. However, the hold capacitor can not be charged instantaneously to the full input voltage. In the two-diode topology, the time constant charging the hold capacitor depends on the current from the strobe pulse generator. Therefore, a strong clock buffer is required to optimize the circuit performance. The sampling pulses are generated by an SCFL differential delay chain coupled to an OR gate as shown in Fig. 6 [8]. A sinusoidal LO input of approximately 0 dBm is amplified, and the delayed edges of the LO produce positive and negative sampling pulses as illustrated in the timing diagram. The generator produces strobes with fixed pulsewidths at different LO frequencies. The simulated pulsewidth values of approximately 350 ps give enough time for the circuit to set up the track mode when the switches are on with the designed clock buffer. Thus, the duty cycle at 500-MHz sampling frequency is 0.18 that gives theoretical conversion loss of 2 dB. Except in the clock buffer, standard SCFL cells with resistor loads are used to avoid the effects of uncorrelated process variations between enhancement and depletion transistors. The clock buffer shown in Fig. 7 amplifies the pulse swing above the diode turn on point and feeds sufficient current to the bridge. Because of

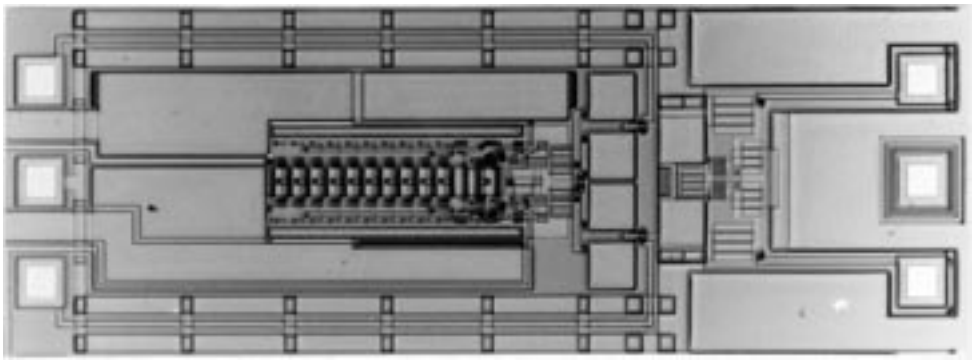


Fig. 9. Microphotograph of the chip. The differential RF input signal is brought to chip via pads on the left side and isolated from the clock circuitry in the middle with symmetrical analog ground planes on both sides of the input wires.

the capacitive coupling to the bridge, only the relative swing between the positive and negative branch is important, relaxing the absolute dc-level requirements with low supply voltages. In this case transistor loads are required in the intermediate stage to produce sufficient amplitude swings.

D. Layout and Fabrication

The circuit has been fabricated using Vitesse semiconductor 0.6-μm E/D-MESFET process designed for digital VLSI circuits [9]. The process did not support inductors, and the capacitors built from three wiring layers had small capacitance per-unit area and large parasitics to substrate. The capacitors were implemented using a "sandwich structure" shown in Fig. 8 to minimize the area and parasitics. The top and bottom metal layers were connected together forming two parallel capacitors with the middle plate. The coupling capacitors between diode bridges and clock buffer require special attention because the parasitic capacitance from the signal nodes to ground is unavoidable. The parasitic capacitance from the bottom plate to the substrate is of the order of 50% of the capacitance value between two metal layers. By placing the bottom metal on the clock buffer side a significant part of the strobe current will flow to ground ruining the circuit performance. Connected the other way around the parasitics do not have significant effect on the strobe pulse swing and current in the bridge. The photograph of the fabricated circuit is shown in Fig. 9. The active circuit area is 1050 μm$\times$ 500 μm including 77 transistors.

IV. Measurement Setup

Spectral measurements were done to evaluate the circuit performance. A 180° power splitter and biasing blocks were connected between the circuit and the RF synthesizer to produce the differential input. The output was combined with a discrete 180° hybrid. Due to the dc-block in the output, the lower frequency limit was fixed at 100 kHz in the measurements, and direct conversion performance must be evaluated based on this very low IF. Most of the measurements were done at 5-MHz IF output. A separate synthesizer using the crystal reference from the RF source generated the LO for the sampler. Noise figure measurements of a subsampling mixer must be also done with a spectrum analyzer because

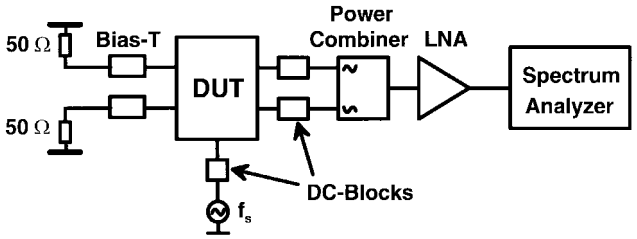


Fig. 10. The noise measurement setup. Low noise amplifier is required to raise the measured noise over the internal level of the spectrum analyzer.

the large number of harmonics and different mixing principles interfere with the operation of a noise figure meter in the mixer measurement modes, and thus, the results are not reliable. Many modern spectrum analyzers have a separate noise spectral density measurement mode that is accurate and takes into account the filtering in the analyzer itself, for example. Often, the internal noise of the spectrum analyzer exceeds the output noise of the device under test, and a separate low-noise amplifier is needed to amplify the noise from the DUT up to the measurable range. If the difference between the analyzer noise and the output noise is small the result can be scaled to correspond to the desired noise value when the internal noise floor is known

$$N_{\mathrm{DUT}} = N_{\mathrm{SP}} + 10\log_{10}\left(10^{\frac{N_M - N_{\mathrm{SP}}}{10}} - 1\right) - G_{\mathrm{LNA}} \quad (10)$$

where N_M is the measured value including both circuit, N_{DUT}, and spectrum analyzer noise, N_{SP}, in dBs. G_{LNA} is the gain of the low noise amplifier. The noise measurement setup is shown in Fig. 10. The noise figure of the downconverter is calculated by definition from the measured output noise, circuit gain and -174 dBm/Hz input noise spectral density introduced by the 50-Ω termination.

V. Results

The circuit met the design objectives of 2-GHz input bandwidth with small conversion loss, and the measurements matched well with the simulations. The input response is defined to a fixed IF in Fig. 11 at 500-MHz sampling frequency. To achieve sufficient resolution in the measurements at relatively small sampling rates, the LO frequency is adjusted to the closest possible value that produces the desired IF when the RF is swept over the band. The input response follows

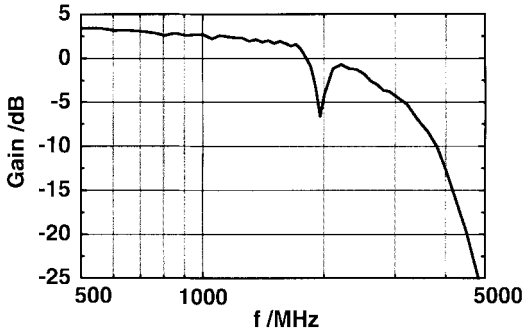


Fig. 11. Input bandwidth of the sampler. The system gain is measured at fixed 5-MHz IF. The sampling frequency is approximately 500 MHz producing the desired IF when RF signal, shown in the x-axis, is varied.

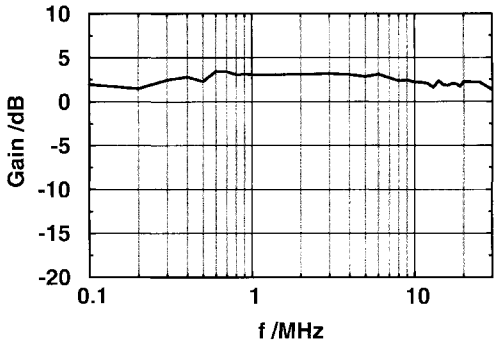
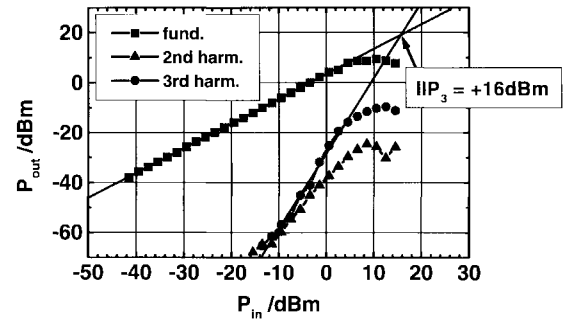


Fig. 12. The IF response of the sampler. The bandwidth is limited by the dc-block and power splitter in the measurement system.

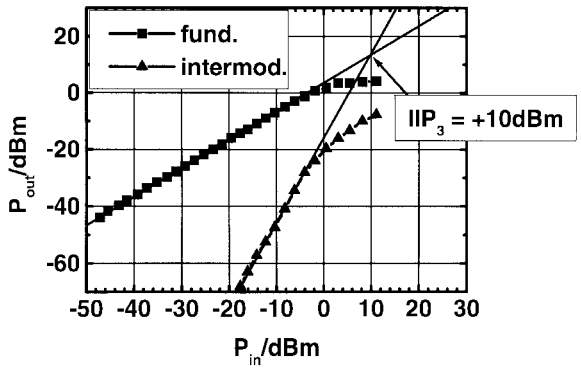
the transfer characteristics of a low pass filter. The notch at 2 GHz is due to the imperfections of the probe card used in measurements. This means that the mixer is capable of operation at two or more different frequency bands using the same system configuration. Of course, the system requires separate preselection filters, and to minimize the noise, the input bandwidth must be restricted up to the highest frequency band. The IF band of the circuit was limited by the external configuration in the measurement system. The IF frequency selection does not have a significant effect on the conversion gain over the measured range shown in Fig. 12.

We measured the circuit with two different LO-frequencies of 500 MHz and 100 MHz. The results are summarized in Table I. The 1-dB conversion loss is small for a passive structure and shows good correspondence with theory and simulated performance. The slightly smaller system gain at the 100-MHz sampling frequency is the effect of signal droop during the longer hold period. The linearity has been measured both with one and two input tones, Fig. 13. The former yields results comparable to [2] and the latter is normally used to specify the intermodulation performance of a mixer. High linearity has been achieved when compared to typical integrated continuous-time mixers. The compression point of $+7$ dBm is close to the theoretical maximum of the topology defined by the diode turn on caused by the input signal swing.

The circuit can operate with a large range of sampling frequencies from 40 MHz to 1.5 GHz, and the minimum required LO input power is only -2 dBm. The LO power fed to the sampling bridges is spread over the harmonics of the



(a)



(b)

Fig. 13. (a) Harmonic behavior of the circuit in the single-tone measurement. Input signal at 1005 MHz is downconverted with 500-MHz LO giving 5-MHz IF output and its harmonics at 10 MHz and 15 MHz. (b) Intermodulation test with two-tones. The downconverted replicas are at 5 MHz and 6 MHz and intermodulation products at 3 MHz and 7 MHz. All the measured harmonics are within the sampler IF bandwidth.

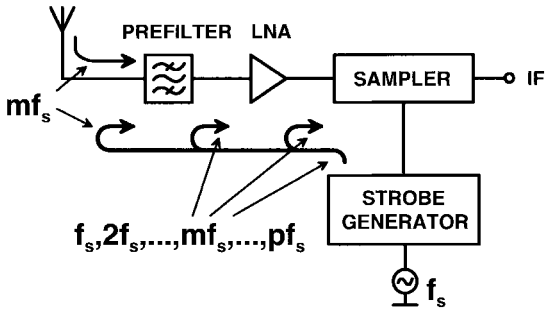


Fig. 14. In direct conversion receivers all harmonic leakage from the strobe pulse generator to the circuit input will self-mix in the downconverter if reflected back before the preselection filter. The external distortion and reflections from the antenna will be filtered, and only the component located at the detected channel will convert over the desired frequency.

sampling frequency in the strobe pulse generator. The spectrum depends mainly on the digital clock circuitry including the buffering. The LO harmonics that leak to the circuit input can be divided into two categories whether the component is located inside or outside of the prefilter passband in the receiver front-end described in Fig. 14. The LO leakage to the RF input is measured, and different harmonics are summed to give the total leakage power at 100 and 500 MHz as -64 and -56 dBm, respectively. In direct conversion receivers, self-mixing is a serious problem because the mixing product will be located at baseband together with the received signal

TABLE I
MEASURED CIRCUIT PERFORMANCE

f_{LO}	500 MHz	100 MHz
RF Input Bandwidth	2.0 GHz	1.6 GHz
System Gain	3 dB	2 dB
Sampler Gain	-1 dB*	-2 dB*
Buffer Gain	4 dB*	4 dB*
Single-Tone		
IIP3	+16 dBm	+19 dBm
-1dB Compression	+7 dBm	+5 dBm
Two-Tone		
IIP3	+10 dBm	+10 dBm
-1dB Compression	-1 dBm	-1 dBm
Noise Figure**	23 dB	29 dB

* Estimates based on simulations
** Output buffer noise excluded

[10]. In a subsampling mixer, all the leaked LO harmonics can self-mix down to baseband if reflected back before the preselection filter, and they can be treated equally at all sampling frequencies. The reflections from the mismatch in the antenna and the power from external reflections or nearby transceivers operating at the same frequency will be filtered out, and all harmonics except the one located at the passband of the preselection filter will be attenuated significantly. Although the internal self-mixing can be stronger, the spurious responses from external sources are more difficult to predict and compensate later with digital techniques. Because the power spreads over a larger number of harmonics, reducing the power-per-component when a lower sampling frequency is used, the low sampling frequency gives even more benefit than the total LO leakage power indicates. In that case the harmonic in the prefilter passband is much smaller than the corresponding component when a high sampling frequency is used. This would compensate for the larger noise figure in certain applications. In our sampler, when operating at 1.5-GHz RF-input, the in-band harmonic leakage will be -61 dBm at 500-MHz sampling frequency and 15 dB smaller at 100 MHz. The difference is approximately the same at other harmonics as well.

The nominal supply voltage is 3 V but the digital supply for the strobe pulse generator can be as low as 2.7 V. The strobe pulse generator dissipates 125 mW of power which is much lower than in some earlier diode bridge samplers [11], [12]. The output buffer needs to drive 50-Ω loads, and therefore consumes 102 mW. For an on-chip load the dissipation would be significantly smaller.

VI. CONCLUSION

We have implemented a diode bridge based subharmonic mixer operating at mobile radio frequencies up to 2 GHz. Small conversion loss for a passive mixer (1 dB) has been achieved with high linearity. The circuit operates from a 3-V power supply and dissipates less power than many other diode bridge samplers. Noise aliasing is an inherent problem in subharmonic sampling, but it can be reduced by using high sampling frequencies. On the other hand, LO leakage to input is smaller at low sampling frequencies which has special significance in direct conversion applications. Subsampling downconverters can replace traditional continuous-time mixers and use a low frequency LO synthesizer in superheterodyne or direct conversion receivers. In the future, sampling downconversion together with other discrete-time analog signal processing and high-speed A/D-conversion techniques is a promising choice for new generation receiver architectures.

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